

0083-0865-2



#2616
7-12-01
Jubro

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF:

Masashi GOTOH, et al.

: EXAMINER: CUNEO, K.

SERIAL NO.: 09/119,626

CPA FILED: January 29, 2001

: GROUP ART UNIT: 2841

FOR: CIRCUIT BOARD HAVING
BONDING AREAS TO BE
JOINED WITH BUMPS BY
ULTRASONIC BONDING

AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

In response to the Official Action dated March 13, 2001, please amend the above-identified application as follows:

IN THE CLAIMS

Claim 13 is amended as follows:

13. (Once Amended) A circuit board comprising:

a main body; and

a conductive layer provided on said main body, said conductive layer having
conductive pattern, said conductive pattern having:

a plurality of bonding areas to where a plurality of bumps of a chip
element are simultaneously joined by ultrasonic bonding; and

RECEIVED
JUL 12 2001
TECHNOLOGY CENTER 2800

at least two grooves located proximate to one of said bonding areas to put the bonding area therebetween, at least a part of said grooves extending a certain direction.

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 7, 9, and 13-15 are presently active in this case, Claim 13 having been amended by way of the present Amendment. Claim 15 has been withdrawn from consideration.

In the outstanding Official Action, the drawings were objected to for not depicting a chip element with bump leads. However, the Applicants respectfully submit the Figures 2 and 3 depict a plurality of bumps (22) provided on a chip (21), thereby satisfying the requirements of 37 CFR 1.83(a). Accordingly, the Applicants submit that a drawing amendment is unnecessary, and respectfully request the withdrawal of the objections to the drawings.

Claim 13 was objected to for a minor informality noted in paragraph 4, on page 2 of the Official Action. Claim 13 has been amended as suggested in the Official Action, and therefore the Applicants respectfully request the withdrawal of the objection to Claim 13.

Claims 7 and 9 were rejected under 35 U.S.C. 102(b) as being anticipated by Yusuke (JP 07263849). For the reasons set forth below, the Applicants respectfully request the withdrawal of this art rejection.

Claims 7 and 9 of the present application recite a circuit board comprising a main body, and a conductive layer provided on the main body. The conductive layer has a conductive pattern having at least one bonding area. The conductive layer having at least one of an isolated notch part and a recess located proximate to and not extending within the at least one bonding area. Claim 7 recites that the notch part or the recess partially narrows the conductive pattern to form a narrow pattern part. Claim 9 recites that the notch part or the recess narrows the conductive pattern at the at least one bonding area.

Regarding the anticipation rejection based upon the Yusuke reference, the Yusuke reference depicts a printed circuit board a joining part of a wiring which makes possible the prevention of short circuit of adjacent wirings and lead pins. The Yusuke reference depicts a wiring (4) formed on a board (3). The wiring (4) includes a joining part (5) to which a lead pin of a semiconductor device is to be joined. A dam (7) is provided so that it surrounds three sides of the periphery of the joining part (5). Accordingly, solder (6) left over in the joining part (5) flows into the space between the joining part (5) and the dam (7) and is prevented from overflowing the dam (7). In the figures of the Yusuke reference, the joining part (5) is depicted as being slightly larger in width than the wiring (4). Additionally, the dam (7) is depicted as a structure separate from the joining part (5).

The Applicants respectfully submit that the Yusuke reference does not disclose or suggest all of the express limitations recited in independent Claims 7 and 9. For example, the Yusuke reference does not disclose or suggest a circuit board having a notch part or a recess that partially narrows the conductive pattern to form a narrow pattern part, as recited in Claim 7. Furthermore, the Yusuke reference does not disclose or suggest a circuit board having a notch part or a recess that narrows the conductive pattern at the at least one bonding area, as

recited in Claim 9. The present application describes a circuit board configuration which enables a chip to be fixedly secured thereto in an even manner with a high bonding strength. The notch part or recess recited in Claim 7 and 9 partially narrows the conductive pattern. The present application notes that the width of the conductive layer surrounding the bonding area greatly affects the ultrasonic bonding conditions. (See page 12, lines 4-10, of the present application.) Accordingly, the inventions recited in Claims 7 and 9 provide a narrow conductive pattern in order to control the bonding conditions of the circuit board, which provides the ability to ensure a consistent bonding strength to thereby overcome deficiencies in the prior art. (See, for example, page 3, lines 19-22 of the present application.)

In contrast to the invention recited in Claims 7 and 9 of the present application, the Yusuke reference describes a joining part (5) that is depicted as being larger in width than the wiring (4). The Yusuke reference further depicts a dam (7), which is configured as a structure separate from the joining part (5) and that surrounds three sides of the periphery of the joining part (5). The dam (7) provides a wall to prevent solder (6) left over in the joining part (5) from flowing to an adjacent wiring thereby short circuiting the adjacent wirings. The Yusuke et al. reference does not disclose or suggest a circuit board having a notch part or a recess that partially narrows the conductive pattern to form a narrow pattern part, as recited in Claim 7. Nor does the Yusuke reference disclose or suggest a circuit board having a notch part or a recess that narrows the conductive pattern at the at least one bonding area, as recited in Claim 9. In fact, as stated above, the joining part (5) is larger than the wiring (4) and the dam (7) is depicted and described as a structure that is separate from the joining part (5) and wiring (4). Accordingly, the Applicants submit that the dam (7) does not teach a notch part or recess that narrows the conductive pattern.

Not only does the Yusuke reference not disclose such a narrowed conductive pattern structure, but the Yusuke reference is concerned with a distinctly different problem than the present invention and therefore does not suggest to one of skill in the art a motivation to modify the Yusuke reference to arrive at the present invention. The Yusuke reference is concerned with providing a structure that will prevent solder from flowing off a joining part to an adjacent wiring thereby short-circuiting the circuit board, while the present invention is concerned with providing a structure that ensure consistent bonding strength.

As the Yusuke reference does not disclose all of the limitations of Claims 7 and 9 of the present application, the Applicants respectfully submit that the Yusuke reference does not anticipate Claims 7 and 9 of the present application. Accordingly, the Applicants respectfully request the withdrawal of the anticipation rejection of Claims 7 and 9.

Claims 13-14 were rejected under 35 U.S.C. 103(b) as being unpatentable over Figure 11 of the present application and Mims (U.S. Patent No. 3,893,223). For the reasons set forth below, the Applicants respectfully request the withdrawal of this art rejection.

Claim 13 of the present application recites a circuit board comprising a main body, and a conductive layer provided on the main body. The conductive layer has conductive pattern. The conductive pattern has a plurality of bonding areas to where a plurality of bumps of a chip element are simultaneously joined by ultrasonic bonding, and at least two grooves located proximate to one of the bonding areas to put the bonding area therebetween, where at least a part of the grooves extend a certain direction.

Regarding the obviousness rejection based upon Figure 11 of the present application and the Mims reference, Figure 11 depicts and the corresponding written portion of the specification describes a circuit board (23) on which chip (21) is placed. The specification

describes ultrasonically bonding the chip (21) provided with bumps (22) on to the circuit board (23) using ultrasonic bonding. The bonding is described as being performed in a simultaneous manner. To the contrary, the Mims reference is directed to an invention that provides a structure that prevents the breaking of adjacent and previously made welds. (See, for example, the abstract; column 2, lines 52-56; and column 3, lines 5-9.) Accordingly, the Mims reference is specifically intended for use in welding processes where individual welds or groups of welds are made, and then a later adjacent weld is made. Accordingly, the Applicants respectfully submit that one of skill in the art would not have been motivated to combine the Mims reference to the device of Figure 11 of the present invention because in Figure 11 the bonding occurs in a simultaneous manner and accordingly there is no risk of breaking a previously made weld. Therefore, one of skill in the art would not have a motivation to look to the Mims reference, since the Mims reference is configured to solve a problem that did not exist for the device depicted in Figure 11.

The Applicants, therefore, respectfully submit that the outstanding obviousness rejection is based on the improper application of hindsight considerations. It is well settled that it is impermissible simply to engage in hindsight reconstruction of the claimed invention, using Applicant's structure as a template and selecting elements from the references to fill in the gaps. *In re Gorman*, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991). Recognizing, after the fact, that a modification of the prior art would provide an improvement or advantage, without suggestion thereof by the prior art, rather than dictating a conclusion of obviousness, is an indication of improper application of hindsight considerations. Simplicity and hindsight are not proper criteria for resolving obviousness. *In re Warner*, 397 F.2d 1011, 154 USPQ 173 (CCPA 1967). Absent the teachings of the present invention, one of skill in the art

would not have been provided with a motivation to combine the Mims reference (which provides a bonding method that ensures that previously made welds are not damaged by subsequent welds) with Figure 11 of the present application (in which the bonds are simultaneously performed).

As there is no teaching of a motivation to combine the cited art, the Applicants respectfully submit that the cited art does not render obvious Claims 13 and 14 of the present application. Accordingly, the Applicants respectfully request the withdrawal of the obviousness rejection of Claims 13 and 14.

Accordingly, the Applicants respectfully submit that the circuit boards recited in Claims 7, 9, 13 and 14 of the present application are distinguishable over the cited references, and therefore the Applicants request the withdrawal of the outstanding art rejections.

Consequently, in view of the above discussion, it is respectfully submitted that the present application is in condition for formal allowance and an early and favorable reconsideration of this application is therefore requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Gregory J. Maier
Attorney of Record
Registration No. 25,599
Christopher D. Ward
Registration No. 41,367



22850

Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 11/98)

GJM/CDW/brf

I:\atty\cdw\0083\0865.am3.wpd

0083-0865-2



| |
|------------------------------------|
| Marked-Up Copy |
| Serial No: <u>09/119,626</u> |
| Amendment Filed on: <u>7-10-01</u> |

IN THE CLAIMS

Please amend Claim 13 as follows:

13. (Once Amended) A circuit board comprising:

a main body; and

a conductive layer provided on said main body, said conductive layer having
conductive pattern, said conductive pattern having:

a plurality of bonding areas to where a plurality of bumps of a chip
[elements] ~~element~~ are simultaneously [jointed] joined by ultrasonic bonding; and
at least two grooves located proximate to one of said bonding areas to
put the bonding area therebetween, at least a part of said grooves extending a certain
direction.

RECEIVED

JUL 12 2001

TECHNOLOGY CENTER 2800